REMARKS

This application has been carefully reviewed in light of the Office Action dated December 14, 2005. Claims 1-22 remain in this application. Claims 1 and 5 are the independent claims. Claims 1, 5, 8 and 14 have been amended. Claims 3 and 15 have been cancelled, without prejudice. Claims 20-22 have been added. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Specification Objections

The abstract was objected to for undue length. In response, the abstract has been amended to comply with MPEP §608.01(b). Reconsideration of the abstract, as amended, is respectfully requested.

The title was objected to for being non-descriptive. In response, the title has been amended to more distinctly describe the invention. Reconsideration of the title, as amended, is respectfully requested.

Art-Based Rejections

Claims 1-2, 5-8, 11-14 and 17-19 were rejected under 35 U.S.C. §102(b) over US 5,822,559 (Narayan); Claims 3, 9 and 15 were rejected under 35 U.S.C. §103(a) over Narayan in view of US 6,260,134 B1 (Zuraski); and Claims 4, 10 and 16 were rejected under 35 U.S.C. §103(a) over Narayan in view of US 2002-0056035 A1 (Rozenshein).

Applicant respectfully traverses these rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Narayan Reference

Narayan discloses a microprocessor having a plurality of early decode units configured to detect double dispatch instructions and to dispatch these instructions to a pair of decode units. Complex instructions are executed serially by an MROM unit, and simple instructions are dispatched to a single decode unit. *(See Narayan, Col. 3, lines 7-14).*

The Zuraski Reference

Zuraski is directed to a predecode unit configured to predecode a fixed number of instruction bytes of variable length instructions per clock cycle. The predecode unit outputs predecode bits which identify whether any of the predecoded instruction bytes are the start byte of an instruction. An instruction alignment unit then uses the start bits to dispatch the variable byte-length instructions to a plurality of decode units that form fixed issue positions within a processor. *(See Zuraski; Col. 2, line 60 to Col. 3, line1).*

The Rozenshein Reference

Rozenshein is directed to an instruction system that includes an instruction root having an operation selection field for selecting an operation to be performed by a data processor and an instruction prefix. *(See Rozenshein; Par. [0024]).*

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device that performs pipeline control.

As defined by independent Claim 1, a data processing device which performs pipeline control includes a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues. The instructions include a given target

instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction. A prefix instruction decoder circuit performs decode processing only on a prefix instruction. The prefix instruction decoder circuit receives the instruction codes of the instructions before decoding that are fetched in the instruction queues, judges whether or not each of the instruction codes is a given prefix instruction, and causes a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction. A general-purpose decoder circuit receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction and decodes the decode instruction. When the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register. The given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction. The prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction. The decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "wherein the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction," as required by amended independent Claim 1. In addition, the applied references do not disclose or suggest, "wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction," as required by amended independent Claim 1. Moreover, the applied references do not disclose or suggest, "wherein the decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction," as required by amended independent Claim 1.

The Office Action concedes that Narayan does not disclose that the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction.

The Office Action purports that Zuraski discloses the use of a prefix instruction that is predecoded (or decoded before the main decoder) in order to simplify circuitry. *(See Zuraski; Col. 13, line 65 to Col. 14, line 1).*

However, Zuraski discloses that, because the instruction length is variable, the multiplexer must be able to shift the instruction bytes suitably (in order to adjust a variety of instruction lengths), which increases the complexity of the

multiplexer. By predecoding a fixed number of instruction bytes, the multiplexer processes the instruction bytes. *(See Zuraski; Col. 2, lines 49-57; Col. 3, lines 1-5)*. Thus, Zuraski fails to disclose the features of amended Claim 1. Even though Zuraski discloses shifting an instruction code, Zuraski fails to shift an execution result of a target instruction, as recited in the claims of the present invention. Moreover, Zuraski discloses shifting the positions of instruction bytes for adjustment, but fails to disclose storing shift information necessary for shifting execution results of the target information in the target instruction modifying information register nor shifting the information stored in the target instruction modifying information register, as recited in the claims of the present invention.

In contrast to Narayan and Zuraski, the claims of the present invention require that the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction. The prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction. The decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction. Accordingly, the present invention performs predetermined pipeline control for operation processing in which execution results of a target instruction are shifted arithmetically or logically and, thus, has an objective which is different from those of the cited references.

Narayan and Zuraski, alone or in combination, do not disclose or suggest these features of the present invention as required by amended Claim 1, and Rozenshein does not remedy the deficiencies of Narayan and Zuraski.

Since the applied references do not disclose or suggest the above features of the present invention as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that amended independent Claim 5 is allowable for at least the same reasons as discussed above in reference to amended independent Claim 1 and such allowance is respectfully requested.

The remaining claims depend either directly or indirectly from amended independent Claims 1 and 5 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

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If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: March 10, 2006

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